

REMARKS

The Examiner objected to the disclosure. In response, Applicants have amended the specification as suggested by the Examiner.

The Examiner objected to claims 1 and 12-15. In response, Applicants have amended claims 1 and 12-15 as suggested by the Examiner.

The Examiner rejected claims 1, 2, 4, 5, 10, 11, 12, 13, 15, 16, 21 and 22 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Koze (4,687,682) in view of Kiyosumi *et al.* (4,603,059; hereinafter, "Kiyosumi").

The Examiner rejected claims 3 and 14 under 35 U.S.C. §103(a) as allegedly being unpatentable over Koze (in view of Kiyosumi) as applied to claims 1 and 12 above, and further in view of Moslehi *et al.* (5,296,385; hereinafter "Moslehi").

The Examiner rejected claims 6-9 and 17-20 under 35 U.S.C. §103(a) as allegedly being unpatentable over Koze (in view of Kiyosumi) as applied to claims 5 and 16 above, and further in view of Sugino (5,121,705).

Applicants respectfully traverse the §103 rejections with the following arguments.

35 U.S.C. §103(a)

Claims 1, 2, 4, 5, 10, 11, 12, 13, 15, 16, 21 and 22 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Koze (4,687,682) in view of Kiyosumi *et al.* (4,603,059; hereinafter, "Kiyosumi").

Applicants respectfully contend that claims 1 and 12 are not unpatentable over Koze in view of Kiyosumi, because Koze in view of Kiyosumi does not teach or suggest each and every feature of claims 1 and 12.

For example, Koze in view of Kiyosumi does not teach or suggest the feature of "forming a substructure comprising the material **sandwiched between a topside** of the first semiconductor wafer and a **backside** of a portion of the second semiconductor wafer" (emphasis added).

The Examiner argues: "Koze discloses a method of fabricating semiconductor wafer 100 (Fig. 1), comprising:...the material sandwiched between a topside of the first semiconductor wafer and a backside of a portion of the second semiconductor wafer (note Col. 1, lines 44-63, i.e., a capping layer comprising silicon dioxide and silicon nitride is formed on the backside of the wafers prior to epitaxially growing a layer on the front sides of the wafers)".

In response, Applicants respectfully contend that Koze in Col. 1, lines 44-63, does not teach or suggest forming a substructure that includes a material **sandwiched between a topside** of a first wafer and a **backside** of a second wafer as taught by Applicant's claims 1 and 12. In contrast, Koze in Col. 1, lines 44-63 teaches "a "cap" formed on a backside of a wafer ". Applicants contend that Koze (i.e., in Col. 1, lines 44-63) does not disclose that a material is **sandwiched between a topside** of a first wafer and a **backside** of a second wafer.

Furthermore, Koze teaches in col. 3, lines 1-3, " Referring to FIG. 1, silicon wafers (100 are placed by pairs into wafer boats (101), so that the **active** face of one wafer **contacts** the **active** face of another ". Therefore, Applicants contend that Koze teaches away from Applicants claims 1 and 12 because Koze teaches an **active** face of one wafer **contacting** an **active** face on another wafer and therefore the Koze invention cannot comprise a material located **between a topside** (i.e., an active side) of a first wafer and a **backside** (a non-active side) of a second wafer as taught by Applicant's claims 1 and 12. Applicants define a "topside" of a wafer (i.e., in paragraph 0019) as follows: " The term " topside" of a semiconductor wafer (e.g., topside 8 of the semiconductor wafer 4 and topside 12 of the semiconductor wafer 7) is defined herein including in the claims as a surface of a semiconductor wafer that **comprises** or will comprise (i.e., through a wafer/semiconductor device manufacturing process) **active electrical components** (e.g., transistors, resistors, capacitors, etc.) and/or conductive wiring between active electrical components ". Additionally, Applicants define a "backside" of a wafer (i.e., in paragraph 0019) as follows: " The term "backside" of a semiconductor wafer (e.g., backside 10 of the semiconductor wafer 4 and backside 15 of the semiconductor wafer 7) is defined herein including in the claims as a surface of a semiconductor wafer that **does not comprise active electrical components** (e.g., transistors, resistors, capacitors, etc.)".

Based on the preceding arguments, Applicants respectfully maintain that claims 1 and 12 are not unpatentable over Koze in view of Kiyosumi, and that claims 1 and 12 are in condition for allowance. Since claims 2-11 depend from claim 1 and claims 13-22 depend from claim 12, Applicants contend that claims 2-11 and 13-22 are likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account No. 09-0456.

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